



1/4" NTSC/PAL CMOS Image Sensor with 640x480 Pixel Array

PC7080S

Rev 0.0

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▶ Features

- ▷ 648 x 488 Effective pixel array with RGB bayer color filters and micro-lens.
- ▷ Power supply : HVDD/CVDD/AVDD=3.3V
- ▷ Input. Clock Frequency : 27MHz
- ▷ Output formats
 - ◆ Composite Output mode - CVBS (NTSC/PAL)
- ▷ Image processing on chip lens shading, gamma/defect/color correction NR (2D noise reduction), color interpolation, edge enhancement, brightness, contrast auto black level, auto white balance auto exposure control and back light compensation
- ▷ High Image Quality And Ultra low light performance
- ▷ I2C master include
- ▷ Horizontal / Vertical mirroring
- ▷ Automatic flicker cancellation
- ▷ Software Reset
- ▷ Crystal input support
- ▷ On chip regulator for DVDD
- ▷ CLCC Package type supports

Pixel Size	5.60 um x 5.60 um
Effective Pixel Array	648 (H) x 488 (V)
Effective Image Area	3.6288 mm x 2.7328 mm
Optical Format	1/4 inch
Input Clock frequency	27Mhz
Frame Rate	60 field / sec @ NTSC 50 field / sec @ PAL
Dark Signal	49.6 [mV/sec] @ 60°C
Sensitivity	12.5 [V/Lux.sec]
Power Supply	Analog : 3.3V HVDD : 3.3V CVDD : 3.3V DVDD : 1.62V (Ext. LDO)
Power Consumption	272 mW @ Dynamic_NTSC 297 mW @ Dynamic_PAL
	428 uW @ Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 105 [°C]
Dynamic Range	62 [dB]
SNR	46 [dB]

[Table 1] Typical Parameters

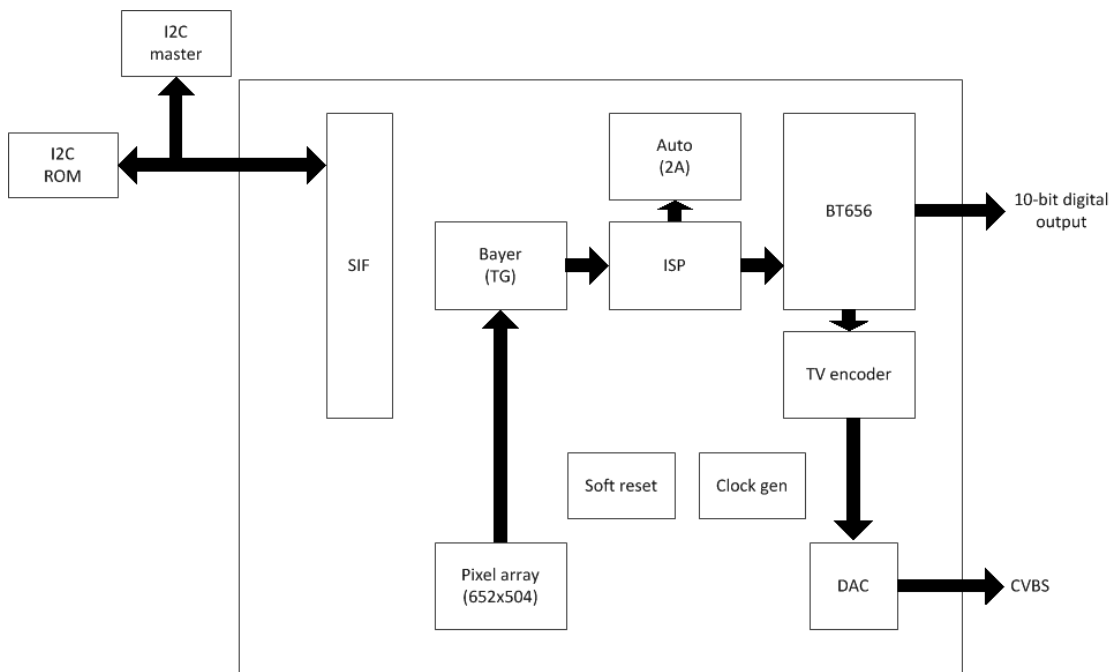
▶ Signal Environment

PC7080S don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended, it may flow leakage current by shot circuit path in the input PADS.

▶ Chip Architecture

PC7080S has 648 x 488 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time processing blocks to produce YCbCr 4:2:2 output data. Image signal processing includes such operations such as gamma correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. BT656 formatter supports 10-bits digital output and TV encoder supports CVBS analog output.

Internal functions and output signal timing can be changed by modifying registers directly via 2-wire serial interface called I2C or by programming the internal/external ROMs which contain device settings.



[Fig. 1] Block Diagram



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